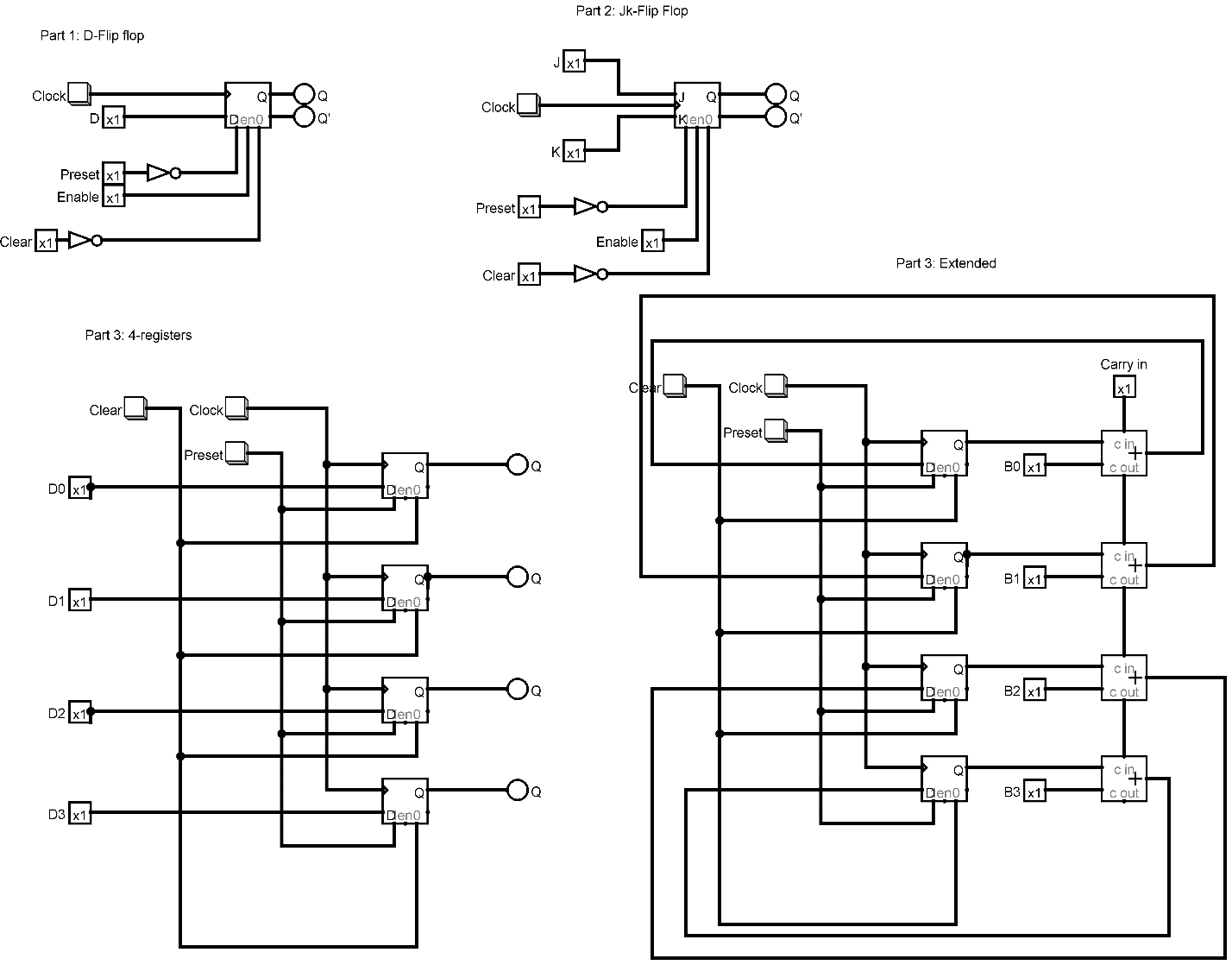
Lab 4 report



1. D Flip Flop

In the part 1, we will use a D Flip flop with Rising edge on Trigger. On the Clock input we will need a Clock signal; therefore a button is used to generate the signal and is attached to the D Flip flop. A pin is used for the input D and is connected to the D Flip Flop. Preset and Clear input is connected to the D flip flop on its respectable positions, both have a one pin Not Gate on its path to the D Flip flop. Another input Enable is connected to the D Flip Flop. Enable input is used to determine if data from input is loaded to D Flip Flop on clock’s edge. If Enable is set to 0 or false, it will ignore the clock and will retain its state. Two outputs, Q and Q’ are connected to the D Flip Flop, Q will display the current input and Q’ will store the input D on clock’s edge. Example, if we set Preset, Enable and Clear to 1, and if we give input D as 1 and click on the button, the Q will display that input 1 as will the LED turn red showing its 1 . And then if we change the input D to 0 and click the Clock button again, Q’ output will store the previous input, and the Q will be faded and Q’ LED will turn on since previous input was 1.

1. JK Flip Flop

Like D flip flop but this time instead of D input, J and K input will be on the JK Flip Flop. On the Clock input we will need a Clock signal; therefore, a button is used to generate the signal and is attached to the JK Flip Flop. Preset and Clear input is connected to the JK flip flop on its respectable positions, both have a one pin Not Gate on its path to the JK Flip flop. Another input Enable is connected to the JK Flip Flop. Enable input is used to determine if data from input is loaded to D Flip Flop on clock’s edge. If Enable is set to 0 or false, it will ignore the clock and will retain its state. The JK flip flop is basically a gated SR flip-flop with the addition of a clock input circuitry that prevents the illegal or invalid output condition that can occur when both inputs S and R, are equal to logic level “1”.

1. 4 registers And Extension ALU

One clock button is used to connect to the four D flip flops. Similarly, same Preset and Clear buttons are used and connected to the four D flip flops. Four inputs D0, D1, D2 and D3 are connected separately to the D flip flops. Four output LEDs,Q0,Q1,Q2 and Q3 are connected to the D flip flops separately .If Preset button is used , it will set all the outputs of the D flip flop to 1, and all the Q1 Q2 Q3 Q4 will turn on and the LED will red. Clear will set all the output LED to 0 and they will be faded. If any of the input D0-D3 is set to 1 and then clock signal from the Clock button is given, the respective Q will be turned on and will show the LED red on the output.

For the Extension of the 4 register to Alu, the difference is that , the four outputs of the four D flips flop will be one of the input of the 1 bit adder, therefore for four output we will need four 1 bit adder, with 1 data bits. For the adders we will also need a Carry in input, which we will connect to one of the adders and will connect the other adders by its c out pin to other adder’s c in pins. Since we are using adders to add, we will need another set of inputs, therefore input B0-B3 will be connected to the respective adders.

The sum output of the adders will be connected to the inputs of the D flip flops to retain its state and used to the addition of the bits.